Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of Claims:

1-20. (Cancelled)

21. (Currently Amended) A method, for use in a digital communication system, for interleaving input data having K≥2 bits according to an interleaving scheme into an interleaved sequence, said method comprising the steps of:

a) storing the input data in a first memory means;

b) generating first indices of N succeeding bits of the interleaved sequence;

c) converting, according to an inverse of said interleaving scheme, said first indices into second indices indicative of the positions where said N succeeding bits of the interleaved sequence are stored in said first memory means; and,

d) reading out said N succeeding bits from said positions in said first memory means, thereby generating at least part of said interleaved sequence;

wherein N is selected to have a value of K/M with $M \geq 2$ denoting a sub-sampling factor, and wherein said first memory means is adapted to generate an output sequence representing one of M polyphases of said interleaved sequence when said N succeeding bits are read out from said positions.

22. (Previously Presented) The method according to claim 21, wherein:

said first memory means is organized in a matrix form comprising rows and columns;

said first indices comprise first row indices and first column indices; and,

said second indices comprise second row indices and second column indices; and, wherein said step of converting comprises the steps of:

converting said first row indices into said second row indices so that inter-row permutation operations according to said interleaving scheme are performed when said step of reading out is executed; and,

converting said first column indices into said second column indices so that intra-row permutation operations according to said interleaving scheme are performed when said step of reading out is executed.

23. (Previously Presented) The method according to claim 22, wherein said step of converting said first row indices comprises the steps of:

storing at least one permutation pattern defining said inter-row permutation operations in a second memory means; and,

addressing said second memory means with addresses depending on at least said first row indices, causing said second memory means to output said second row indices.

24. (Previously Presented) The method according to claim 22, wherein said step of converting said first column indices comprises the step of:

converting said first column indices and said second row indices into said second column indices so that intra-row permutation operations depending on a row index are performed when said step of reading out is executed.

25. (Previously Presented) The method according to claim 24, wherein said step of converting said first column indices comprises the steps of:

determining base sequence indices depending on said first column indices and said second row indices by adding index increments depending on said second row indices to previously determined base sequence indices; and,

determining said second column indices on the basis of at least said first column indices and said base sequence indices.

26. (Previously Presented) The method according to claim 25, wherein said step of converting comprises the steps of:

storing at least said index increments in a third memory means;

storing at least one base sequence specified by said interleaving scheme in a fourth memory means; wherein,

said step of determining base sequence indices is adapted to address said third memory means so as to read therefrom said index increment; and,

said step of determining said second column indices is adapted to address said fourth memory means so as to read therefrom corresponding values of said at least one base sequence.

27. (Previously Presented) The method according to claim 21, wherein N is selected to have a value of K, and wherein said first memory means is adapted to generate said interleaved sequence when said N succeeding bits are read out from said positions.

28. (Cancelled)

29. (Previously Presented) The method according to claim 21, wherein said steps of generating and converting are executed, at least partially, before said step of storing.

30. (Currently Amended) An interleaving apparatus, for use in a digital communication system, for interleaving input data having $K \geq 2$ bits according to an interleaving scheme into an interleaved sequence, said apparatus comprising:

a) an index generator for generating first indices of N succeeding bits of the interleaved sequence;

b) an index conversion unit connected to said index generator for converting, according to an inverse of said interleaving scheme, said first indices into second indices indicative of the positions where said N succeeding bits of the interleaved sequence are stored in a first memory means; and,

c) first memory means connected to said index conversion unit, wherein said first memory means is adapted to store said input sequence and to generate at least part of

said interleaved sequence when said N succeeding bits are read out from said positions;

wherein N is selected to have a value of K/M with $M \geq 2$ denoting a sub-sampling factor, and wherein said first memory means is adapted to generate an output sequence representing one of M polyphases of said interleaved sequence when said N succeeding bits are read out from said positions.

31. (Previously Presented) The interleaving apparatus according to claim 30, wherein:

said first memory means is organized in a matrix form comprising rows and columns;

said first indices comprise first row indices and first column indices;

said second indices comprise second row indices and second column indices; and, wherein said index conversion unit includes:

a row index conversion unit for converting said first row indices into said second row indices so that inter-row permutation operations according to said interleaving scheme are performed when said N succeeding bits are read out from said positions in said first memory means; and,

a column index conversion unit for converting said first column indices into said second column indices so that intra-row permutation operations according to said interleaving scheme are performed when said N succeeding bits are read out from said positions in said first memory means.

32. (Previously Presented) The interleaving apparatus according to claim 31, further comprising:

second memory means for storing at least one permutation pattern defining said inter-row permutation operations: and,

wherein said row index conversion unit includes addressing means for addressing said second memory means with addresses depending on at least said first

row indices, thereby causing said second memory means to output said second row indices.

33. (Previously Presented) The interleaving apparatus according to claim 31, wherein said column index conversion unit comprises:

means for converting said first column indices and said second row indices into said second column indices so that intra-row permutation operations depending on a row index are performed when said N succeeding bits are read out from said positions in said first memory means.

34. (Previously Presented) The interleaving apparatus according to claim 33, wherein said column index conversion unit includes:

first processing means for determining base sequence indices depending on said first column indices and said second row indices by adding index increments depending on said second row indices to previous base sequence indices;

second processing means, connected to said first processing means, for determining said second column indices on the basis of at least said first column indices and said base sequence indices determined by said first processing means.

35. (Previously Presented) The interleaving apparatus according to claim 34, further comprising:

third memory means, connected to said first processing means, for storing at least said index increments;

fourth memory means, connected to said second processing means, for storing at least one base sequence specified by said interleaving scheme; wherein:

said first processing means is adapted to address said third memory means so as to read therefrom said index increments; and,

said second processing means is adapted to address said fourth memory means so as to read therefrom corresponding values of said at least one base sequence.

36. (Previously Presented) The interleaving apparatus according to claim 30, wherein N is selected to have a value of K, and wherein said first memory means is adapted to generate said interleaved sequence when said N succeeding bits are read out from said positions.

37. (Cancelled)

38. (Currently Amended) The interleaving apparatus according to claim [[37]] 31, comprising:

$M \geq 2$ interleaving units, each adapted to receive said input sequence and to generate an output sequence representing a different one of said M polyphases;

a combiner connected to said M interleaving units for combining the output sequences generated by said M interleaving units into said interleaved sequence; and,

a control unit for controlling the operations of said M interleaving units and said combiner.

39. (Previously Presented) The interleaving apparatus according to claim 38, further comprising:

fifth memory means, connected to said M inter-leaving units, for storing at least one of a complete set of base sequences according to the interleaving scheme and a complete set of base sequence index increments.

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